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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/731,060	12/07/2000	Edward Colles Nevill	550-192	1332

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EXAMINER	
ZHEN, LI B	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,060	NEVILL ET AL.	
	Examiner	Art Unit	
	Li B. Zhen	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 16 are pending in the application.

CLAIM INTERPRETATIONS

2. The broadest reasonable interpretations of the claims have been afforded that instant application. The following are interpretations of the claimed invention.

Examiner notes that claim 1 does not require the scheduling support logic to manage scheduling between threads or task irrespective of whether a preceding program instruction was executed by the said hardware based execution unit or said software based execution unit. The last limitation of claim 1 recites "said hardware based execution unit includes scheduling support logic operable to generate a scheduling signal for triggering scheduling operation to be performed between program instructions". Therefore, the scheduling support logic only generates the signal to trigger the scheduling operation. The scheduling operation as defined in the claims is not required to be part of the hardware based execution unit. In fact, according to applicant's specification, the scheduling operation is performed by scheduling code that is identified as software [see Fig. 10, element 76; p. 26, line 30 – p. 27, line 3 and p. 27, lines 16 – 26]. The last limitation of claim 1, in view of applicant's specification, is interpreted as follows: the hardware based execution unit includes scheduling logic to generate a scheduling signal to trigger a scheduling operation performed by scheduling code. The scheduling code (software), manages scheduling between threads or tasks irrespective of whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,937,193 to Evoy [cited in the previous office action] in view of U.S. Patent No. 6,374,286 to Gee et al. [hereinafter Gee].**

6. As to claim 1, Evoy teaches the invention substantially as claimed including an apparatus [computer system 10, Fig. 1; col. 3, lines 29 – 42] for processing data operable to execute operations specified in a stream of program instructions [converting platform-independent instructions to be executed by a processor into corresponding

native instructions for the processor; col. 4, lines 9 – 20 and col. 3, lines 42 – 60], the apparatus comprising:

(i) a hardware based instruction execution unit operable to execute program instructions [a translation circuit 50 coupled to system data bus 24 is utilized to receive 8-bit Java bytecodes and output corresponding 32-bit native instructions directly to processor 40 for execution; col. 4, lines 52 – 62]; and

(ii) a software based instruction execution unit [software interpreter; col. 5, lines 57 – 67] operable to execute program instructions [interpret the unmapped bytecode via a software interpreter; col. 5, lines 57 – 67, col. 6, lines 1 – 8, col. 7, lines 8 – 16]; wherein

(iii) program instructions to be executed are sent to the hardware based execution unit [a platform-independent instruction (here a Java bytecode) is fetched from the memory; col. 10, lines 45 – 57] for execution [Translate Code routine 200, for translation state machine 153; col. 32 – 45]; and

(iv) program instructions received by the hardware based execution unit for which execution is not supported by the hardware based execution unit are forwarded to the software based execution unit for execution [If no corresponding native instruction exists, table 51 outputs an exception signal, which notifies processor 40 that software interpretation of the bytecode may be required; col. 7, lines 8 – 17; col. 5, lines 57 – 67; col. 6, lines 1 – 8; col. 9, lines 54 – 65; col. 11, lines 23 – 37] with control being returned to the hardware based execution unit for a next program instruction to be executed [selecting next bytecode; col. 7, lines 8 – 16; col. 11, lines 6 – 15].

7. As to scheduling support logic, Evoy schedules instructions to be executed by the processor and dispatching the next instruction to be executed [After execution of a native instruction when in the platform-independent mode, processor 40 increments its address counter to the next instruction, which has the effect of selecting the next bytecode provided to byte select multiplexer 56; col. 7, lines 17 – 28]. However, Evoy does not specifically disclose scheduling operation for managing scheduling between threads or tasks irrespective of whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit.

However, Gee teaches hardware based execution unit [JEM processor 100, Fig. 1; col. 8, line 58 – col. 9, line 5], software based execution unit [processor opcodes will trap to software to resolve the class reference and replace the null CSA ptr; col. 13, lines 50 – 56], and scheduling support logic to generate a scheduling signal for trigger a [partition interval timer 1712 is used to signal the completion of a partition time slice and return to JVM0 operation, which, as previously mentioned, checks for system events and schedules the next partition; col. 28, lines 43 – 52] scheduling operation [thread scheduling software; col. 21, lines 25 - 57] for managing scheduling between threads or tasks [In the inventive JEM processor, a priority-based scheduler which conforms to the above-described rules dispatches (makes ready to execute) the highest priority thread from the set of all runnable, or "ready", threads; col. 21, lines 43 – 58] irrespective of whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit [decision concerning which thread to run at any particular moment is made in accordance with a scheduling policy, col. 21,

lines 25 – 60; Examiner notes that Gee discloses scheduling of threads according to a scheduling policy and not based on whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Gee and Envoy because Gee's teachings provide a conventional JAVA scheduling policy is defined in the JAVA Language Specification that implements a preemptive, priority-based scheduling policy [col. 21, lines 27 – 36 of Gee] and allows threads with the highest priority to execute first in a real-time embedded system [col. 21, lines 47 – 50 of Gee].

8. As to claim 16, this is a method claim that corresponds to apparatus claim 1; note the rejection to claim 1 above, which also meet this method claim.

9. As to claim 2, Evoy teaches the scheduling support logic includes a counter with a value [address counter; col. 7, lines 17 – 27] that is changed in response to a program instruction sent to the hardware based execution unit [After execution of a native instruction when in the platform-independent mode, processor 40 increments its address counter to the next instruction; col. 7, lines 17 – 27].

10. As to claim 3, Evoy teaches the counter triggers generation of said scheduling signal when a predetermined count value is reached [END reserved code; col. 10, line 65 – col. 11, line 6].

11. As to claim 4, Evoy teaches the counter may be programmed to start from a user programmable start value [translation vector base address register 172 stores the starting address of the first table; col. 9, lines 27 – 47].

12. As to claim 5, Evoy teaches the counter counts up to said predetermined value [processor 40 increments its address counter to the next instruction; col. 7, lines 15 – 28].

13. As to claim 6, Evoy as modified by Gee teaches the counter counts down to said predetermined value [partition interval timer 1712; col. 28, lines 43 – 52 of Gee; examiner notes that a timer is a counter that can count up or down to a predetermined value. Therefore, the interval timer corresponds to the timer.].

14. As to claim 7, Evoy as modified by Gee teaches a debug operation is triggered by the scheduling signal [col. 11, lines 22 – 38 of Evoy and col. 26, lines 17 – 30 of Gee].

15. As to claim 8, Evoy does not teach timer logic. However, Gee teaches timer logic operable to generate a timer signal indicative of a time since a last scheduling operation [partition switch time-out watchdog timer 1716; col. 29, lines 12 – 29 of Gee]. It would have been obvious to a person of ordinary skilled in the art at the time the invention was made to combine the teachings of Gee and Evoy because Gee's teachings prevent one thread from taking over the system by refusing to relinquish control [col. 23, lines 18 – 30 of Gee].

16. As to claim 9, Evoy as modified by Gee teaches the scheduling signal is combined with said timer signal to trigger said scheduling operation [partition switch time-out watchdog timer 1716 is used to unconditionally terminate partition execution when the partition interval timer interrupt (1804) is not acknowledged; col. 29, lines 12 – 29 of Gee].

17. As to claim 10, Evoy as modified by Gee teaches a scheduling operation is triggered upon generation of said scheduling signal after said timer signal has reached a predetermined value indicating a predetermined period time since a last scheduling operation has expired [col. 29, lines 12 – 29 of Gee].

18. As to claim 11, Evoy teaches a processor core operable to execute operations as specified by instructions of a first instruction set [col. 4, lines 38 – 44 and col. 7, lines 50 – 61].

19. As to claim 12, Evoy teaches the hardware based instruction execution unit includes an instruction translator [a hardware-implemented translation circuit; col. 4, lines 9 – 20] operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of the first instruction set [if a corresponding native instruction to the selected bytecode exists, table 51 outputs it over data lines 54a and directly to processor 40; col. 7, lines 8 – 16].

20. As to claim 13, Evoy teaches (i) at least one instruction of the second instruction set specifies a multi-step operation that requires a plurality of operations that may be

specified by instructions of the first instruction set in order to be performed by the processor core [translation state machine 153 handles exception conditions by testing for an EXC code. Upon receipt of this code, control is passed to block 212 where the translation process is halted, the REQ signal is released, and an interrupt is sent to processor 140; col. 11, lines 22 – 38]; and

(ii) the instruction translator is operable to generate a sequence of translator output signals to control the processor core to perform the multi-step operation [multiple IMM codes may be required, with separate processing, to handle immediate data of different lengths; col. 11, line 36 – col. 12, line 5].

21. As to claim 14, Evoy teaches the software based execution unit is a software based interpreter [software interpreter; col. 5, lines 57 – 67].

22. As to claim 15, Evoy teaches the program instructions are Java Virtual Machine instructions [col. 4, lines 52 – 62].

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,338,160 discloses an implementation of Java using a Data Resolution Field within a constant pool entry.

U.S. Patent No. 6,332,215 discloses a hardware Java accelerator to implement portions of a Java Virtual Machine.

CONTACT INFORMATION

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on 571-272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2194

LBZ